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FIG. 1
(PRIOR ART)

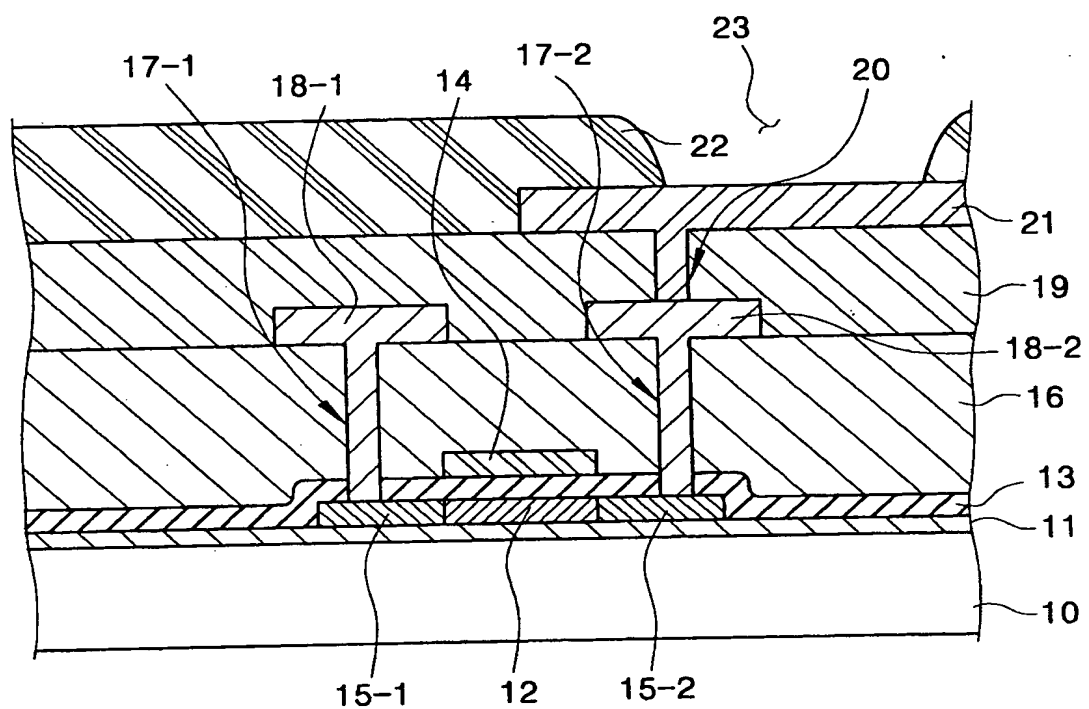


FIG. 2A

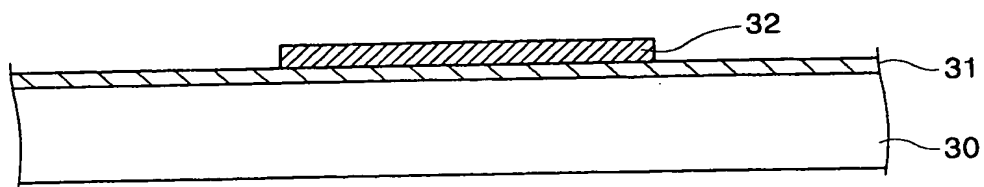


FIG. 2B

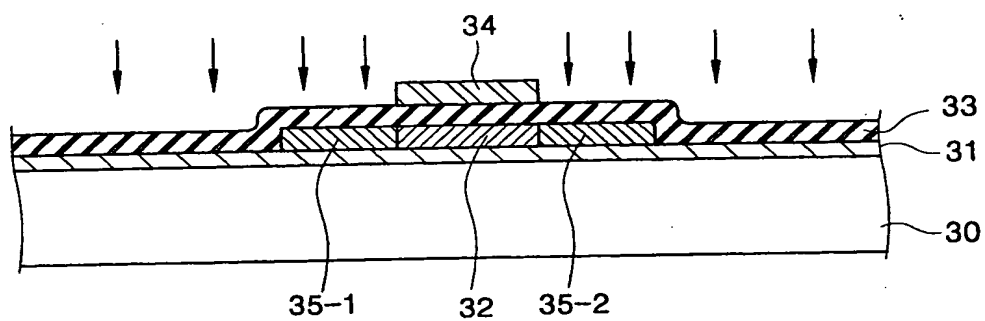


FIG. 2C

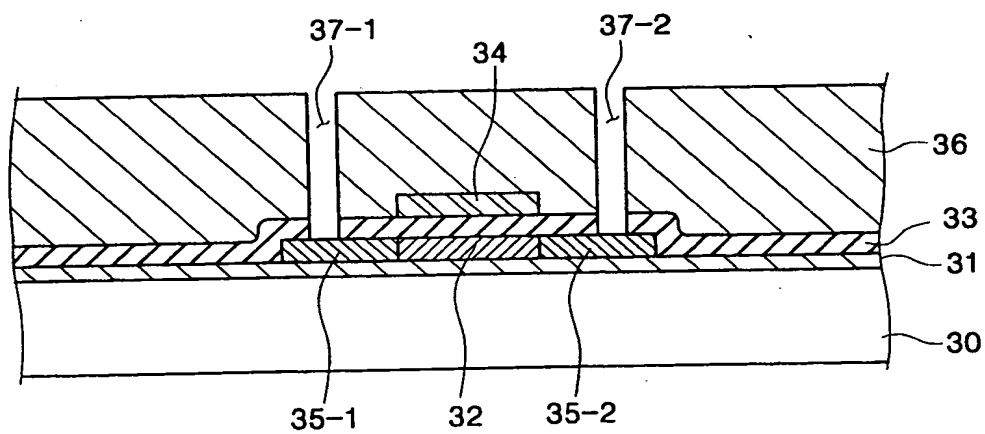


FIG. 2D

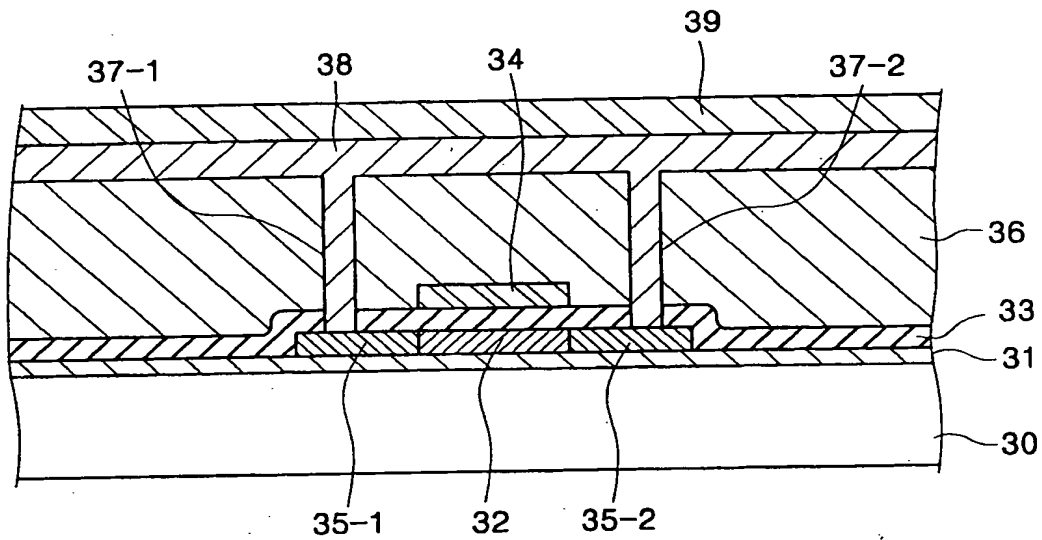


FIG. 2E

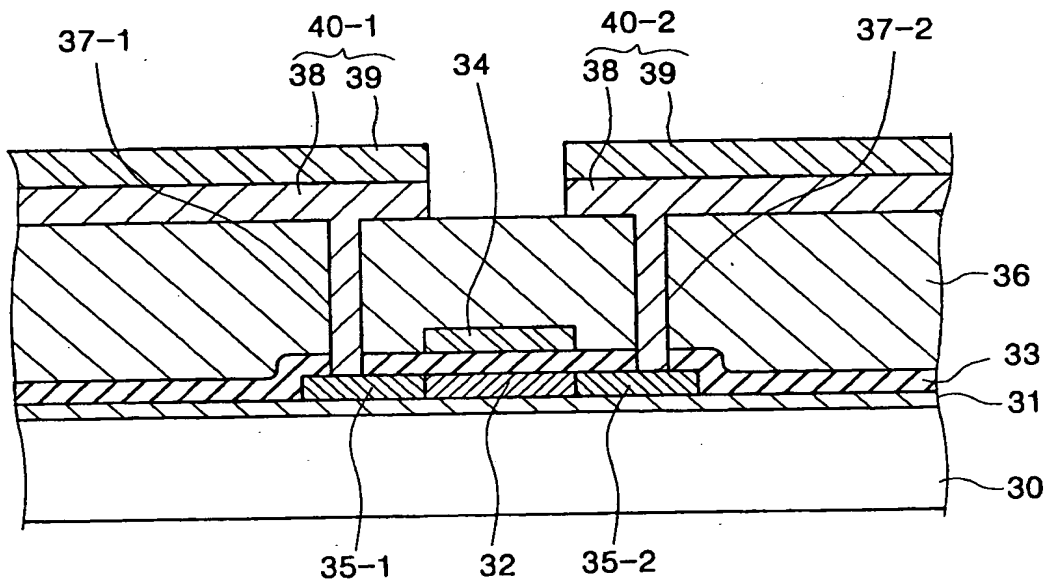


FIG. 3A

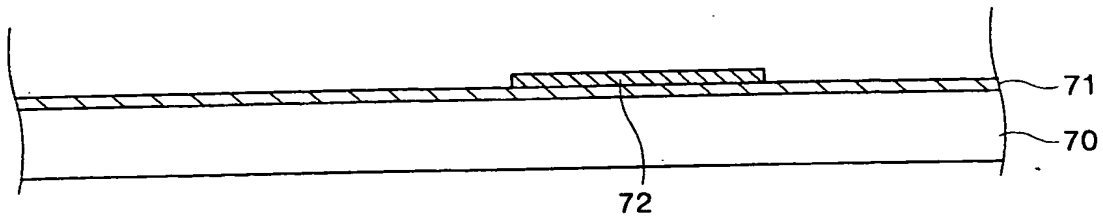


FIG. 3B

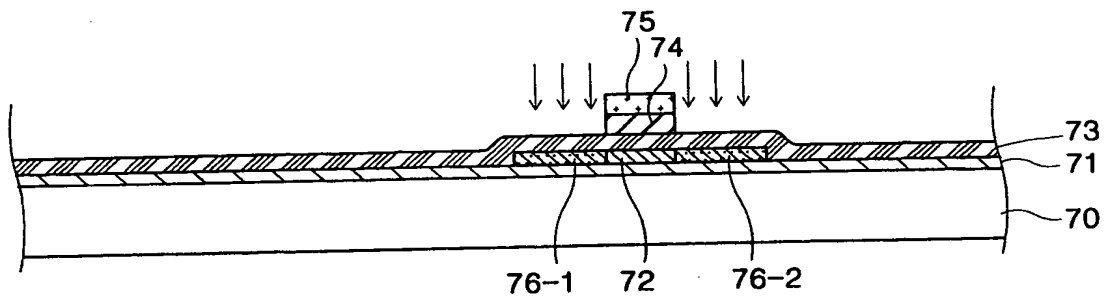


FIG. 3C

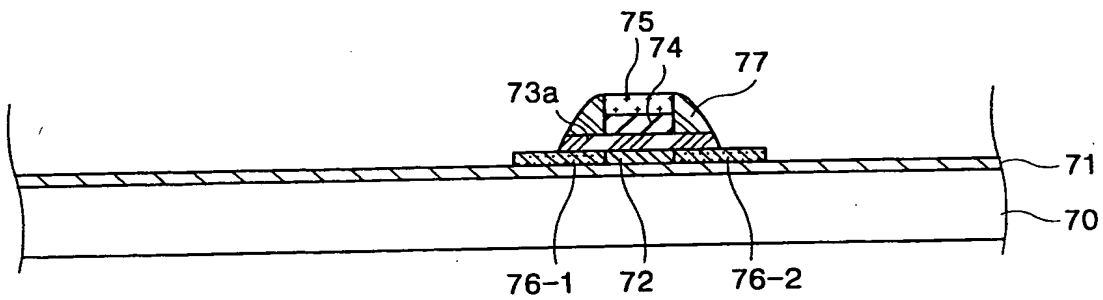


FIG. 3D

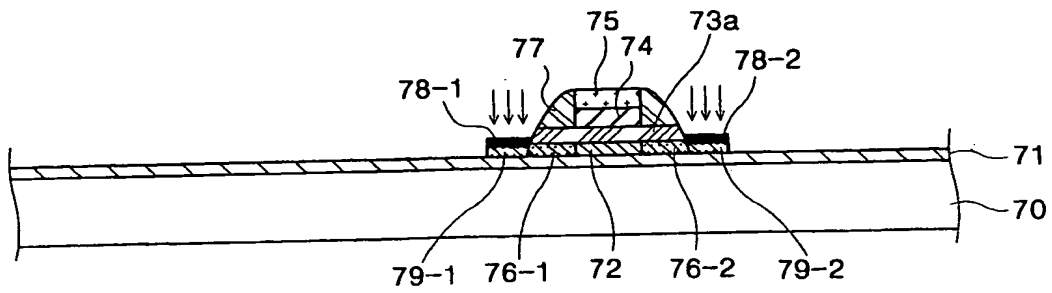


FIG. 3E

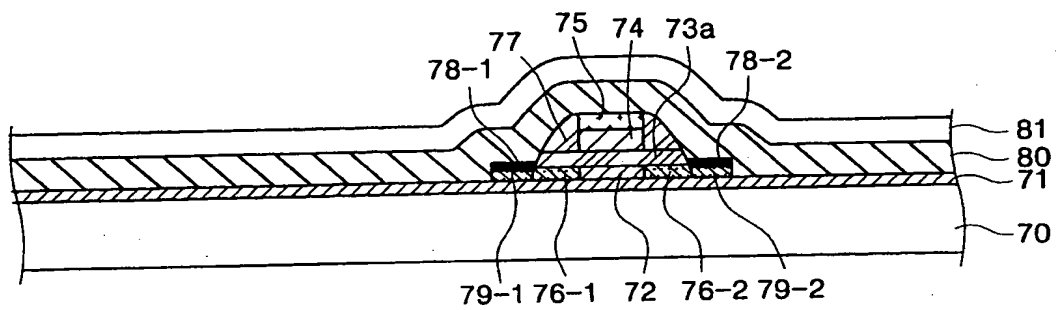


FIG. 3F

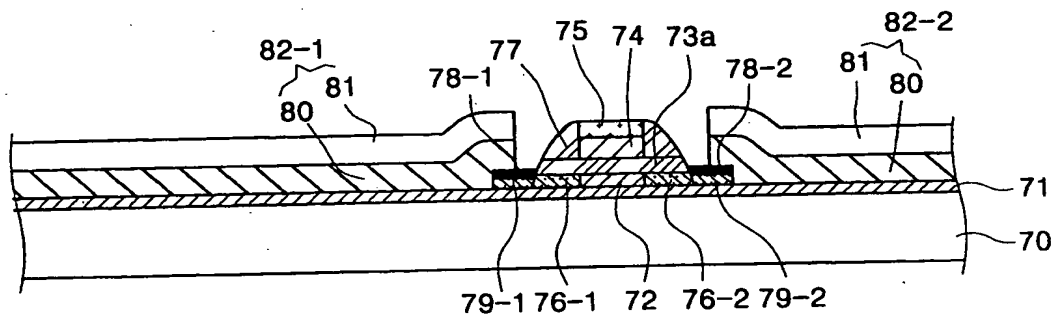


FIG. 4A

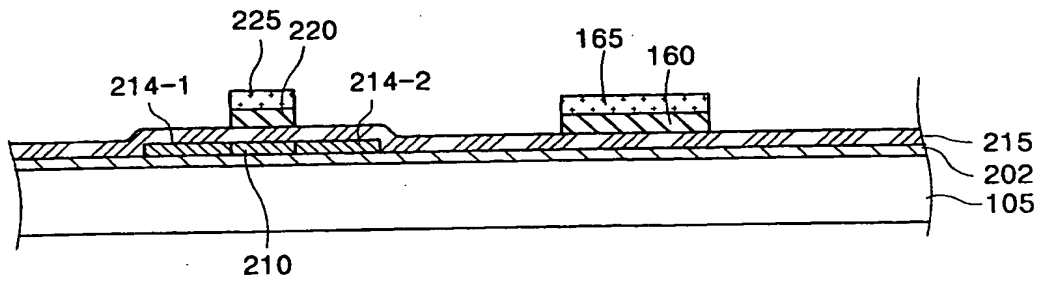


FIG. 4B

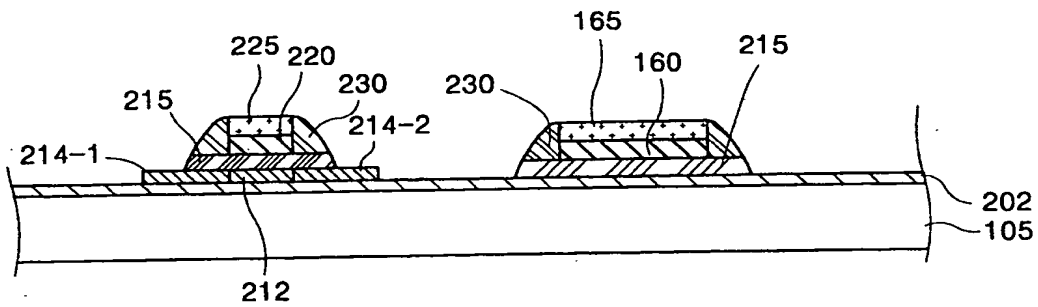
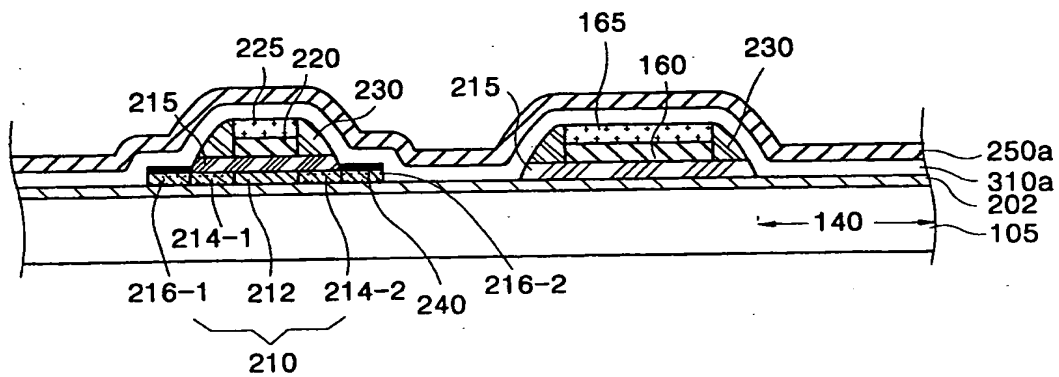


FIG. 4C



A detailed cross-sectional view of a semiconductor device. The device consists of a substrate 105 with a base layer 202. A series of layers and features are built on top, including a layer 140. A bracket 150 groups a central structure 170, which includes a layer 165 and a feature 160. Other features include a series of raised structures 215, 220, 225, 230, 240, 250a, and 310a. A bracket 210 groups a series of layers 212, 214-1, 214-2, 216-1, and 216-2. A bracket 250 groups a series of layers 250a and 310a. A dimension line 140 indicates a length across the device.

This cross-sectional view illustrates a semiconductor device. A substrate 105 is at the base, with a base layer 202 on top. A patterned layer 250 is formed on the base layer, consisting of regions 250a and 310a. A central region 210 contains a structure with layers 212, 214-1, 214-2, 216-1, and 216-2. Other features include 150, 160, 165, 170, 220, 225, 230, 240, 255, 260, and 265.

[illegible]

FIG. 5A

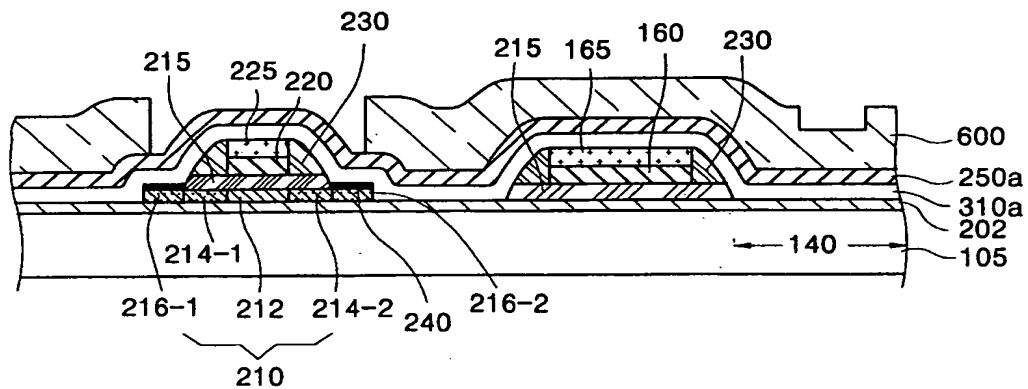


FIG. 5B

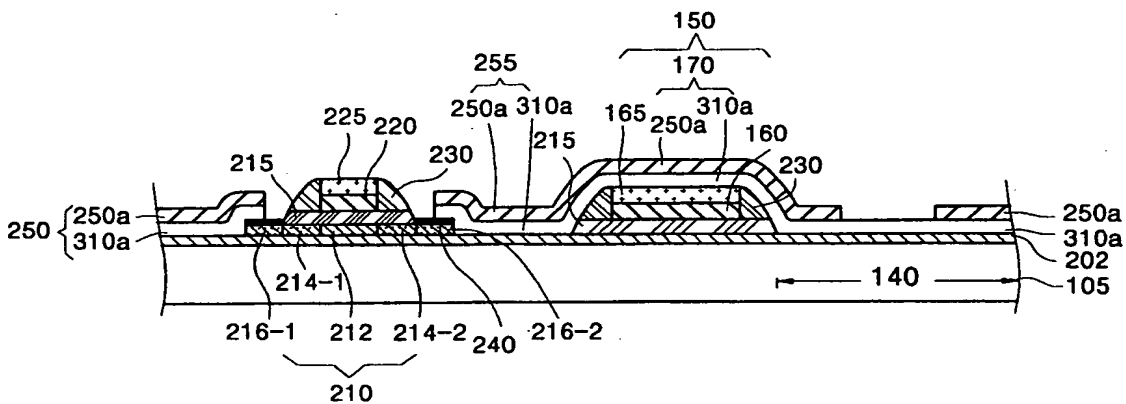


FIG. 5C

